IN THE SPECIFICATION:

Paragraph beginning at page 1, line 11 has been amended as follows:

Connection portions (referred to hereinafter as [[VIA]] VIAs) formed from the upper and lower metal wiring layers of intersection portions of metal wiring layers and from interlayer connecting portions that form connections between metal wiring layers, which are created using EDA tools for automatically placing and wiring in a semiconductor device, are generally formed across the entire surface of the intersection portions. As is shown in the plan view in FIG. 10 and in the cross sectional views along the lines XX' and YY' in FIG. 11, if the upper and lower metal wiring layers M1 and M4 are connected skipping more than one metal layer arranged between the metal wiring layers, the adjacent metal wiring layers M1 and M4 or the metal layers M2 and M3 (M1 and M2, M2 and M3, M3 and M4) are connected using [[VIA]] VIAs, and what is known as a stack VIA (referred to below as an SVIA) structure for connecting the target metal wiring layers M1 and M4 is employed. These SVIA are also arranged in a matrix formation, with the pitches of the wiring tracks T2 and T3 (the pitch in the X direction of T2=PX, the pitch in the Y direction of T3=PY) that are determined by design rules in terms of the layout, extending across the entire surface of the intersection portion 100 (having the surface area W1 × W4) between the lower metal wiring layer M1 having the width W1 and the upper metal wiring layer M4 having the width W4.

Paragraph beginning at page 3, line 30 has been amended as follows:

However, in the SVIA of the above described conventional technology, because the intermediate metal layers (i.e., M2 and M3 in FIG. 11) are provided such that they overlap with the entire area of the intersection portion 100 of the metal wiring layers M1 and M4 that need to be connected, the problem arises that the signal wiring and the like wired using the intermediate metal layers M2 and M3 is not able to pass through the intersection portion 100. In particular, when the metal wiring layers M1 and M4 are formed from wide wires such as those used for power supply wiring, the intersection portion 100 also ends up occupying a large surface area. The problem also arises that the signal wire tracks T2 and T3 of the metal layers M2 and M3 are blocked over the entire surface of this area making it impossible to increase the wiring efficiency. Moreover, as the degree of miniaturization and the level of integration of semiconductor devices advance and the multiplying of the number of metal layers M develops, the number of blocked signal wire tracks also increases correspondingly. Consequently, this problem becomes a factor in preventing the degree of miniaturization and the level of integration of semiconductor devices from advancing. The above is a problem that arises when the intermediate metal layers M2 and M3 are present overlapping the intersection portion 100 of the metal wiring layers M1 and M4. Furthermore, the problem is not limited to this and the same type of problem also arises when intermediate metal layers M2 and M3 are arranged in a configuration where they bridge the gap between metal wiring layers M1 and M4 that do not have an intersection portion so as to form an SVIA.